REMARKS

Applicant appreciates the time taken by the Examiner to review Applicant's present application. This application has been carefully reviewed in light of the Official Action mailed November 29, 2005 ("Office Action"). Claims 1, 7-12, 20-21 and 25 were canceled previously. Claims 32-33 have been added. No new matter has been added. Applicant respectfully requests reconsideration and favorable action in this case. It is noted that the Office Action erroneously refers to the Schwartz reference as U.S. Patent No 6,347,234. U.S. Patent No 6,347,234 is a patent issued to Scherzer. The Schwartz reference is actually U. S. Patent No. 6,434,115.

Rejections under 35 U.S.C. § 103

Claims 13-19, 22-24 and 26-31 stand rejected as obvious over U.S. Patent No. 6,434,115 ("Schwartz") in view of U.S. Patent No. 6,781,984 ("Adam") and U.S. Patent No. 5,126,999 ("Munter").

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). *See* MPEP § 2143 - §2143.03 for decisions pertinent to each of these criteria.

The cited art, Schwartz, Adam, and Munter, do not teach or suggest all limitations of the pending claims separately or in combination. For at least this reason, the cited art cannot be used to establish a case of prima facie obviousness against the pending claims as set forth in detail below.

Claims 13-19

Pending independent claims 13-19 each describe an ingress edge unit. For example, independent claim 13 recites:

> An ingress edge unit configured to be coupled to a data switching matrix, wherein the ingress edge unit comprises:
> one or more ingress ports, each of which is configured to be coupled to an ingress data line;
> a switch coupled to the one or more ingress ports; and
> a plurality of buffers coupled to the switch,
> wherein the switch is configured to store data received via the one or more ingress ports in the plurality of buffers, wherein the data stored in each of the plurality of buffers is destined for a corresponding one of a plurality of destinations; and
> wherein the ingress edge unit is configured to:
> transmit data from each of the plurality of buffers in a corresponding predetermined time slot,
> schedule data from each of the plurality of buffers to be delivered to the corresponding one of the plurality of destinations, independent of the predetermined time slot, and
> receive the data as one or more optical data signals, wherein the one or more optical data signals comprise light having multiple wavelengths.

Independent claims 14, 16, and 19 also recite ingress edge units having similar features. For example, each independent claim 13, 14, 16, and 19 recites "a switch coupled to the one or more ingress ports; a plurality of buffers coupled to the switch; wherein the switch is configured to store data received via the one or more ingress ports in the plurality of buffers, wherein the data stored in each of the plurality of buffers is destined for a corresponding one of a plurality of destinations, and wherein the ingress edge unit is configured to transmit data from each of the plurality of buffers in a *corresponding predetermined* time slot." Thus, the claimed ingress edge unit includes a switch configured to store data according to destination, where data is stored in buffers which correspond to specific destinations. Further, the claimed ingress edge unit is configured to transmit data from each of the buffers according to time slot, where each buffer has a corresponding time slot. Each claimed buffer is configured to correspond to a time slot, and each buffer has a corresponding destination. Accordingly, it follows that data may be transmitted to each destination during a pre-determined time slot corresponding to that destination.

The claimed features are supported by the Specification. The Specification recites in paragraphs [0030-0034], "switch 23 is configured to convey the data received from network

interface cards 21 to selected ones of buffer units 25 ... Switch 23 is configured to provide grooming and routing functions..." The claimed ingress edge unit is configured to enable the switch to route data from the ingress ports to the buffers. The data is received at the ingress port and subsequently routed by the claimed switch prior to storage in a buffer. Each claimed buffer stores data corresponding to a particular destination. Paragraph [0011] recites, "[t]he destination corresponding to each of the [data] cells is identified, and the cells are forwarded to corresponding buffers, wherein each buffer contains only [data] cells which are to be forwarded to the same destination...*Each buffer is read during a corresponding time slot,* and all of the data read out of the buffer is forwarded to the corresponding destination." The Specification recites in paragraphs [0047-0048], "[t]he data contained in these buffers is read out of each buffer sequentially ... *each buffer has a corresponding, dedicated time slot* in each subframe during which data will be read out of the buffer." Finally, in paragraph [0050], the Specification recites, "[b]ecause all of the [data] cells in a given time slot are destined for the same egress edge unit, all of these [data] cells are delivered by the optical switching matrix to that egress edge unit. The [data] cells in subsequent time slots maybe delivered to that same egress edge unit, or to any other egress edge unit (keeping in mind that all of the [data] cells in a particular time slot will be delivered to the same egress edge unit.)" Therefore, the instant invention recites data stored into buffers having corresponding destinations, where each buffer can also have a corresponding time slot to transmit stored data to the destination corresponding to the buffer.

Schwartz does not appear to teach or suggest the claimed ingress edge unit comprising a switch coupled to the one or more ingress ports; a plurality of buffers coupled to the switch; wherein the switch is configured to store data received via the one or more ingress ports in the plurality of buffers, wherein the data stored in each of the plurality of buffers is destined for a corresponding one of a plurality of destinations, and wherein the ingress edge unit is configured to transmit data from each of the plurality of buffers in a *corresponding predetermined* time slot as recited by the pending Claims. In contrast to the claimed ingress edge unit, Schwartz appears to teach a new switching node 11 having a number of input port modules 20(N) and a like number of output port modules 21(N) interconnected by a switching fabric consisting of an inter-port packet switch 22, a packet meta-data processor 23, and a switching node management processor 27 (Schwartz – col. 5, lines 5-15). Schwartz recites, "[f]or each packet received, the input port module 20(n) buffers the packet and identifies from the

destination address contained in the packet's header the appropriate route therefore, in the process identifying the particular output port module 21(n) ... the input port module 20(n) will transfer the packet to the ... packet switch 22. The inter-port packet switch 22, in turn, couples the packet ... to the identified output port module for transmission" (Schwartz – col. 5, lines 21-40). Schwartz also recites, "input port module 20(n) control circuit 33 also receives packet transfer requests from the output port modules 21(n) and, using a packet segment generator 34, controls retrieval and transfer of packets from the packet memory 31 to the inter-port packet switch 22 for transfer to the output port modules 21(n)" (Schwartz – col. 10, lines 30-35). Consequently, Schwartz teaches an input port module which transfers data upon requests from the output port modules instead of transferring data according to a timeslot corresponding to the particular buffer transferring data.

Thus, in contrast to the claimed limitations, Schwartz teaches a system which buffers packets in input port modules without regard to packet destination (i.e., the buffer locations of Schwartz do not appear to correspond to particular outputs), and which transfers data according to requests from the output port modules (i.e., Schwartz does not appear to transfer data according to timeslot, where the timeslot can correspond to individual buffers, and where the individual buffers store data for corresponding destinations). Applicant submits that while the Examiner points to Fig. 2, and lines 5-8, 48-50, 12-17, 15-20, 18-21, 24-29, 21-31, and 32-35 of column 5 and lines 30-35 of column 10 of Schwartz as showing the claimed limitations, examination of these passages fails to illustrate the claimed limitations and, therefore, Schwartz cannot be properly construed as teaching or suggesting the limitations of the pending claims. The Examiner points to Fig. 2, and lines 20-34 of column 3 of Adam as showing claimed limitations, however Applicant submits that the cited passage of Adam fails to remedy the deficiencies of Schwartz with respect to the pending claims. Instead, the cited portions of Adam appear to describe a distributed system having a switch matrix which transmits data in accordance to an idle period control circuit 212 and an output data synchronization control circuit 216. Consequently, the combination of Adam and Schwartz fail to teach or suggest all limitations of the pending independent Claims 13, 14, 16, and 19. Therefore, the cited art does not render the claimed limitations obvious, and independent Claims 13, 14, 16, and 19 are patentably distinct in view of the cited art. Claim 15 is dependent from Claim 14 and Claims 17-18 are dependent from Claim 16. Thus, Claims 15, 17, and 18 are also patentably distinct. For at least these reasons, withdrawal of the rejection of Claims 13-19 is respectfully requested.

Claims 22-24 and 26-31

Pending independent claims 22, 26, 29, 30, and 31 each describe a method for transporting data. For example, independent claim 22 recites:

> A method for transporting data comprising:
> parsing a received data stream into a plurality of data cells;
> identifying a destination corresponding to each of the plurality of data cells;
> segregating the plurality of data cells into distinct sets of data cells, wherein the data cells in each set of data cells has a common destination; and
> sequentially transmitting the sets of data cells to their respective destinations,
> wherein each set of data is transmitted to each destination in a timeslot corresponding to that destination,
> wherein the data stream comprises a plurality of STS1 frames, and
> wherein parsing the received data stream comprises parsing the STS1 frames into data cells.

Similarly, each independent claim 22, 26, 29, 30, and 31 recites "parsing a received data stream into a plurality of data cells; identifying a destination corresponding to each of the plurality of data cells; segregating the plurality of data cells into distinct sets of data cells, wherein the data cells in each set of data cells has a common destination; and sequentially transmitting the sets of data cells to their respective destinations, *wherein each set of data is transmitted to each destination in a timeslot corresponding to that destination.*" Thus, the pending Claims 22-24 and 26-31 each include the features of segregating data cells into distinct sets by common destination and sequentially transmitting the sets of data cells to their respective destinations where each set of data is transmitted to each destination in a timeslot corresponding to that destination.

The claimed features are supported by the Specification. The Specification recites in the abstract, "[e]ach of the buffers is read sequentially during a corresponding timeslot, with the data stored therein being transmitted to the designated egress edge unit." The Specification recites in paragraphs [0047-0048], "[t]he data contained in these buffers is read out of each buffer sequentially ... *each buffer has a corresponding, dedicated time slot* in each subframe during which data will be read out of the buffer." The Specification recites in paragraph [0055], "[e]ach buffer unit is associated with one particular timeslot in a subframe ... The pieces of

data stored in each buffer unit are transmitted to the corresponding destination during the assigned timeslot..." Therefore, each destination may have a corresponding timeslot, and data may be stored into a set of data cells having a common destination for transmission during the timeslot corresponding to that destination.

Schwartz does not appear to teach or suggest the claimed limitations with respect to transmitting data cells corresponding to a respective destination where the data cell is transmitted in a timeslot which corresponds to the destination for the set of data cells. The input modules of Schwartz, in contrast to the claimed invention, appear to send data when the output modules request data. As recited by Schwartz, "[f]or each meta-data packet retrieved by an output port module, the output port module will request that the input port module identified in the meta-data packet transfer the packet identified in the input port module thereto through the packet switch" (Schwartz – Abstract). Thus, it appears the input modules of Schwartz send data when called for by the output module, but not in a predetermined timeslot. This deficiency of Schwartz with respect to the pending claims is not remedied by Adam and/or Munter, as described in further detail below.

The cited portion of Adam does not remedy the deficiencies of Schwartz with respect to the limitations of the pending claims. In particular, Adam appears to teach outputting data "frames under control of idle period control circuit 212 and output data synchronization control circuit 216" (Adam – col. 3, lines 32-34). Further, the cited portions of Munter do not remedy the deficiencies of Schwartz and/or Adam with respect to the limitations of the pending claims. Munter discloses a method and apparatus for input-buffered asynchronous transfer mode switching. However, Munter does not teach or suggest limitations set forth in the pending claims, some distinctions of which are set forth below.

The pending claims include methods of segregating data into data sets where each data set has a common destination, and where the data sets are sequentially transmitted to their respective destinations in a periodic timeslot which corresponds to that destination. In contrast to the claimed limitations, Munter teaches a switching matrix having 'N' input ports. Each input port is buffered by an output-segregated input buffer, and each output-segregated input buffer includes 'N' independent FIFO buffers which store data packets having the same output port destination (Munter, col. 5, lines 28-33). Status of input packets and buffers is reflected dynamically upon an input buffer map. The input buffer map is operated on by an 'N' crosspoint selector to yield a new selection of 'N' crosspoints for each packet cycle on a realtime basis.

(Munter, col. 5, lines 30-48). Thus, it appears the FIFO buffer from which data is sent in a given cycle is arbitrarily determined based on the dynamic load at the switching matrix. Data does not appear to be transmitted from each FIFO " wherein each set of data is transmitted to each destination in a timeslot corresponding to that destination" as claimed by the pending independent Claims. Consequently, the cited art does not teach or suggest the limitations of the pending claims, nor does the cited art provide suggestion or motivation to modify such that the claimed limitations are met. Therefore, the cited art does not render the limitations of independent Claims 22, 26, 29, 30, and 31 obvious. Because Claims 23-24 depend from Claim 22 and Claims 27-28 depend from Claim 26, Claims 23-24 and 27-28 are also patentably distinct. For at least these reasons, withdrawal of the rejection of Claims 22-24 and 26-31 is respectfully requested.

As described above, Claims 13-19, 22-24, and 26-31 are patentably distinct in view of the cited art. Accordingly, withdrawal of the rejections under 35 U.S.C. § 103 is respectfully requested.

Allowable Subject Matter

Claims 2-6 are adjudged to be allowable. Examiner's recognition of patentable subject matter is appreciated.

Added Claims

Claims 32-33 have been added to depend from independent Claim 2 and thus are patentably distinct for at least the same reasons as independent Claim 2. No new matter has been added, and the limitations of the claims are supported by the Specification. In particular, the limitations of Claim 32 are found in paragraph [0052] of the Specification, and the limitations of Claim 33 are found in paragraph [0034] of the Specification.

Applicant has now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims 2-6,13-19, 22-24, and 26-31 in addition to those claims

previously adjudged allowable. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-3183 of Sprinkle IP Law Group.

Respectfully submitted,

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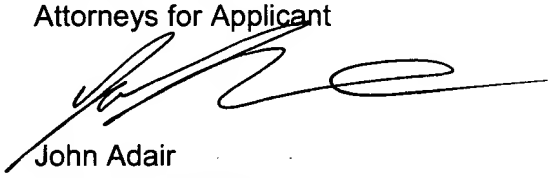

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